Hi,

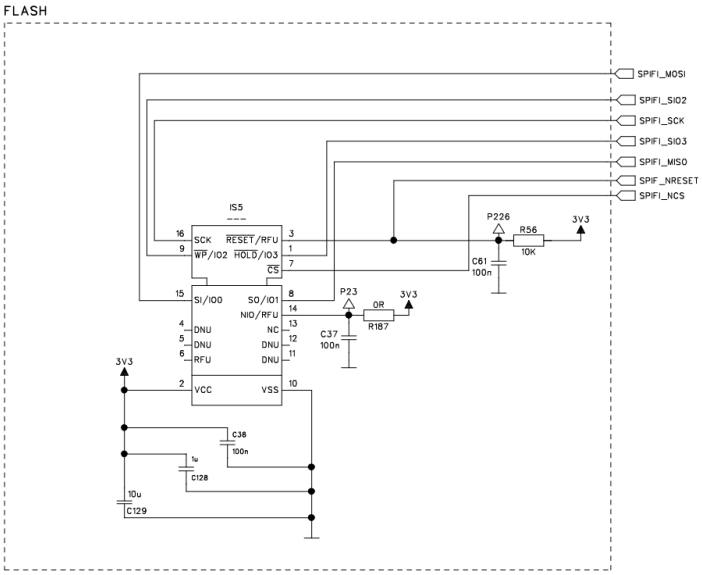
I would like to ask about help with programming external flash issue.

I would like to describe my problem below:

[SETUP]

1. J-Link Plus : HW v10.1, 16-36 (YY – WW), V6.30b;
2. J-Link Base : HW v8.0, 10-04 (YY – WW), V6.30b;
3. J-Flash - SW V6.30b / J-Link commander - V6.30b;
4. J-Flash - SW V6.20e / J-Link commander - V6.20e;
5. NXP LPC1853
6. WINBOND W25Q128FV – Serial flash memory (DUAL/QUAD SPI)
7. Keil uVision for ARM

Our External Flash (6.) connection schematic:



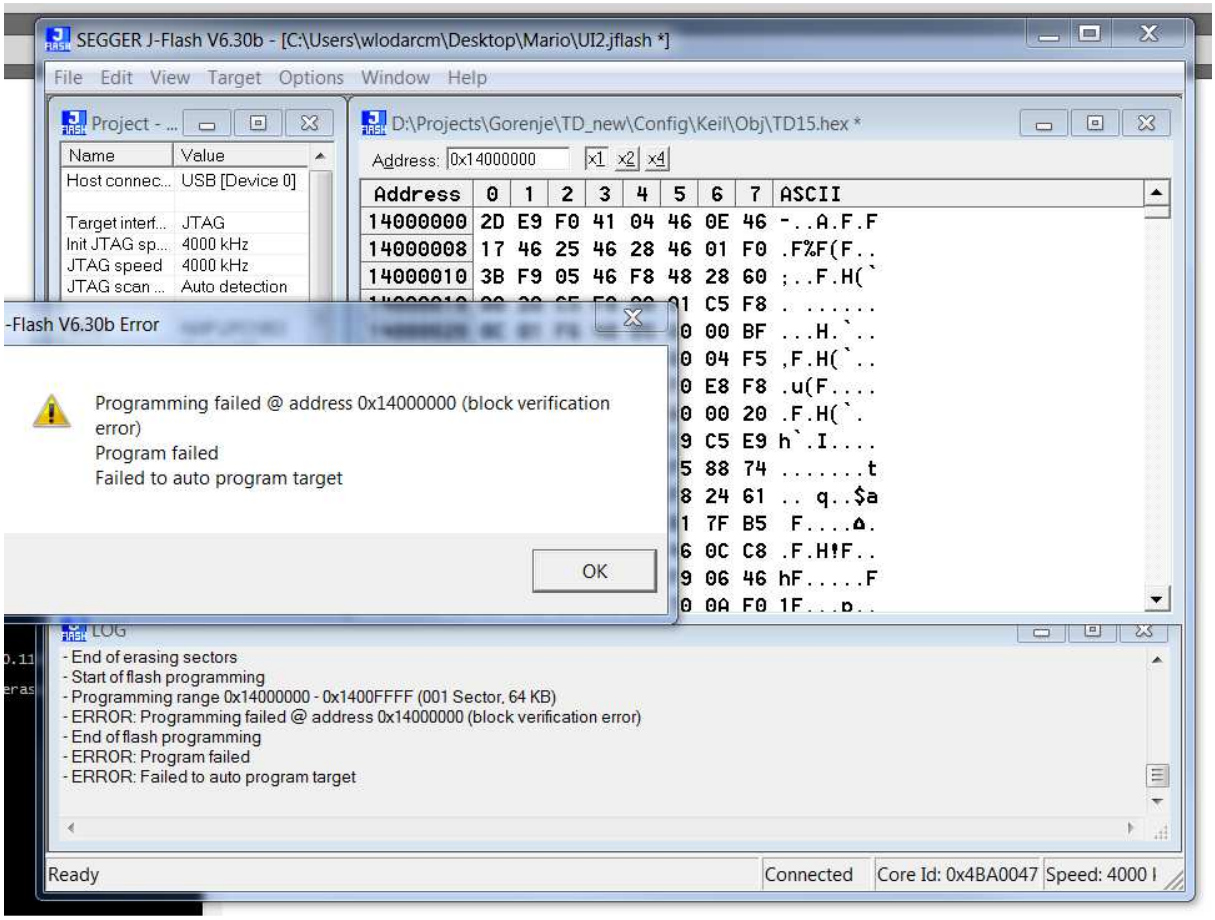
[PROBLEM]

We are programming our PCBs since 2016 with J-Link (at first with v8.0 version and SW v.5.X).
Now we have also the newest J-Link and firmware for that (1. and 2.).
We programed it more than thousand times (with 3. and 4. and older versions). In 99,5% with success.
But sometimes some strange error occur.
Sometimes during programming process, J-Link can not program external flash (6.).
There is problem with access to data block – block verification error.
Sometimes it is not a start address of external flash memory but a hundreds bytes later.

J-Link commander:

```
LPC18xx/43xx reset: Halted CPU before reset.
Unknown LPC18xx/43xx bootloader variant. Halting after reset may fail.

PC = 1A001C6C, CycleCnt = 00000000
R0 = 1A000000, R1 = 1A000000, R2 = 400F1FC0, R3 = 12345678
R4 = 40045000, R5 = 1008000C, R6 = 00000000, R7 = 00000000
R8 = 00000000, R9 = 00000000, R10= 00000000, R11= 00000000
R12= 00000000
SP(R13)= 10008000, MSP= 10008000, PSP= 00000000, R14(LR) = 10405B25
XPSR = 41000000: APSR = nZcvq, EPSR = 01000000, IPSR = 000 (NoException)
CFBP = 00000000, CONTROL = 00, FAULTMASK = 00, BASEPRI = 00, PRIMASK = 00
FPU regs: FPU not enabled / not implemented on connected CPU.

Downloading file [.\Obj\TD15.hex]...
J-Link: Flash download: Bank 0 @ 0x1A000000: 1 range affected (8192 bytes)
J-Link: Flash download: Total time needed: 0.352s (Prepare: 0.049s, Compare: 0.169s, Erase: 0.110s, Program: 0.019s
ify: 0.000s, Restore: 0.002s)
J-Link: Flash download: Restarting flash programming due to program error (possibly skipped erasure of half-way era
ector).
J-Link: Flash download: Skip optimizations disabled for second try.

****** Error: Programming failed @ address 0x14000000 (block verification error)
Error while programming flash: Programming failed.

Reset delay: 0 ms
Reset type NORMAL: Resets core & peripherals via SYSRESETREQ & VECTRESET bit.
LPC18xx/43xx reset: Halting CPU before performing reset...
LPC18xx/43xx reset: Halted CPU before reset.
Unknown LPC18xx/43xx bootloader variant. Halting after reset may fail.


Script processing completed.

"C:\Program Files (x86)\SEGGER\JLink_V630b\JLink.exe"
```

JFlash :



[OUR TEMPORARY SOLUTION]

Before we used *J-Flash* or *J-Link commander,* we had used Keil to program our PCB (with external flash memory algorithm for winbond).
To “fix” our flash, we have to erase flash by **Keil** with flash algorithm written by us (.FLM). Very often it doesn’t work for the first time.
HOW KEIL WORKS : Keil is programming internal NXP memory, and after that, step by step it is coping data from internal memory to external (in the meantime NXP gets new part of data).

After that, we have access to flash again, and now programing with SEGGER tools and J-Link is possible.

We tried to reduce programming speed. It doesn’t work.

[QUESITION]

Could you help us? Do you have any idea what is wrong with our programming procedure? It might be a SW/firmware problem, or rather our HW?
We will be glad for any help.